In the Claims:

Please enter the following amended claim 1:

1. (Five Times Amended) A method of making a flash memory cell including a substrate and a tunnel oxide layer formed on the substrate and a floating gate, the method comprising:

depositing an insulator layer of high temperature oxide directly on exposed portions of the tunnel oxide layer and the floating gate, the insulator layer being deposited to a thickness greater than a thickness of the floating gate, and the insulator layer is formed around vertical surfaces of the floating gate to prevent charge leaking from the floating gate, and wherein the insulator layer of high temperature oxide is formed by a LPCVD process;

polishing the insulator layer to reduce the thickness of the insulator layer and to provide a planar surface that exposes a top surface of the floating gate and the insulator layer; and

depositing an ONO layer on the planar surface directly over the exposed top surface of the floating gate and the insulator layer.

Please cancel claim 3.

Please enter the following amended claims 7 and 23:

7. (Six Times Amended) A method of making a flash memory cell having a substrate and a tunnel oxide layer formed on the substrate, the method comprising:

E2 [forming a first layer of a silicon dioxide on a floating gate of said floating gate transistor;] new matter

Sub G'

depositing a floating gate layer on the tunnel oxide layer to a first thickness;

etching the floating gate layer, to provide a floating gate;

depositing an insulator layer of high temperature oxide directly on exposed portions of the tunnel oxide layer and the floating gate such that the insulator layer has a thickness that is greater than the first thickness, and wherein the insulator layer of high temperature oxide is formed by a LPCVD process;

polishing the insulator layer to provide a planar surface that exposes a top surface of the floating gate and the insulator layer; and

depositing an ONO layer on the planar surface directly over the exposed top surface of the floating gate and the insulator layer.

Sub G'

23. (Thrice Amended) A method of making a flash memory cell including a substrate, a tunnel oxide layer formed on the substrate and a floating gate, the method comprising:

E3

depositing an insulator layer of high quality oxide on the tunnel oxide layer and the floating gate, the insulator layer being deposited to a thickness greater than a thickness of

the floating gate, and the insulator layer of high quality oxide is formed on the vertical surfaces around the floating gate to prevent charge leaking from the floating gate, wherein the high quality oxide is formed by a LPCVD process;

E3 polishing the insulator layer to reduce the thickness of the insulator layer and to provide a planar surface that exposes a top surface of the floating gate and the insulator layer; and

depositing an ONO layer on the planar surface over the exposed top surface of the floating gate and the insulator layer.